SEMICONDUCTOR DEVICE HAVING SUPER JUNCTION STRUCTURE AND METHOD FOR MANUFACTURING THE SAME

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is based on Japanese Patent Application No. 2004-252463 filed on Aug. 31, 2004, the disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to a semiconductor device having a super junction structure and a method for manufacturing the same.

BACKGROUND OF THE INVENTION

[0003] Recently, it is required for a semiconductor device to increase withstand voltage and to reduce on-state resistance. Therefore, a SJ (super junction) structure type semiconductor device is well-known to have high withstand voltage and low on-state resistance. The SJ structure is formed in a drift layer of the device. The drift layer includes an N conductive type column (N column) and a P conductive type column (P column). The N column and the P column compose a unit as a pair of the SJ structure so that multiple pairs of the N column and the P column provide the SJ structure. The N column includes an N conductive type impurity, and the P column includes a P conductive type impurity. Further, the device is composed of a center region and a periphery region. In the center region, a semiconductor switching device is formed. In the periphery region, no semiconductor switching device is formed. Here, the drift layer is disposed from the center region to the periphery region.

[0004] When the device turns off, the N column and the P column in the SJ structure are depleted, respectively, since a depletion layer extending from each P-N junction boundary between the N column and the P column. Thus, the device has high withstand voltage. To deplete the N column and the P column completely and substantially, it is required to equalize impurity amounts of the N column and the P column. Specifically, the impurity amount of the N column is controlled to be equal to the impurity amount of the P column so that both columns are completely depleted. However, in the periphery region, when the impurity amounts of the N column and the P column are equalized, sufficient withstand voltage of the device is not obtained. This is because formation of the depletion layer in the periphery region is different from that in the center region, since a contact region for fixing electric potential of the P column is not formed in the periphery region. Here, in general, the electric potential of the P column is fixed to null, i.e., ground potential. In the periphery region, when the impurity amount of the N column is equalized to that of the P column, the N column and the P column in the periphery region are not sufficiently depleted, compared with the center region. Specifically, the depletion layer of the periphery region is smaller than that of the center region. Accordingly, the total withstand voltage of the device is limited to the withstand voltage of the periphery region. Thus, the withstand voltage of the device is reduced.

[0005] To improve the above problem, a semiconductor device with a periphery region and a center region, which have different impurity amounts, is disclosed in U.S. Pat. No. 6,844,592. Specifically, the P column in the periphery region has an excess impurity amount. In this case, the withstand voltage of the periphery region is improved so that the withstand voltage of the periphery region is equal to that of the center portion. Thus, the total withstand voltage of the device is improved.

[0006] The inventors have further studied about a SJ type semiconductor device. As a result, the inventors found new knowledge as follows. When the N column and the P column in the SJ structure are formed, the impurity amount of each column may be deviated. Specifically, the deviation of the impurity amount is caused by deviation of the impurity concentration and width of each column. The deviation of the impurity amount affects the withstand voltage of the device so that the withstand voltage is extremely reduced. This effect of the deviation is caused in the periphery region in particular. Thus, when the deviation of the impurity amount in the manufacturing process of the device deteriorates the withstand voltage, yielding ratio of product in the manufacturing process is reduced so that the total manufacturing cost increases.

SUMMARY OF THE INVENTION

[0007] In view of the above-described problem, it is an object of the present invention to provide a semiconductor device having a SJ structure. It is another object of the present invention to provide a method for manufacturing a semiconductor device having a SJ structure.

[0008] A semiconductor device includes: a center region, in which a semiconductor switching device is disposed; a periphery region surrounding the center region; and a semiconductor layer including a plurality of pairs of a first column having a first conductive type and a second column having a second conductive type. The semiconductor layer is disposed from the center region to the periphery region. The first and the second columns extend in a thickness direction of the device. The first and the second columns are alternately aligned in a plane perpendicular to the thickness direction of the device. The first column includes a first impurity amount, and the second column includes a second impurity amount. The periphery region includes an utmost outer periphery pair of the first and the second columns and an utmost inner periphery pair of the first and the second columns. The utmost inner periphery pair is disposed next to the center region, and the utmost outer periphery pair is disposed on outmost of the periphery region. The utmost outer periphery pair has a difference between the second impurity amount of the second column and the first impurity amount of the first column, the difference which is smaller than a maximum difference between the second impurity amount and the first impurity amount of another pair of the first and the second columns in the periphery region. The utmost inner periphery pair has a difference between the second impurity amount of the second column and the first impurity amount of the first column, the difference which is larger than a difference between the second impurity amount and the first impurity amount of a pair of the first and the second columns in the center region.

[0009] In the periphery region, the difference of the impurity amount of the utmost inner periphery pair in the periphery region is larger than that of the pair in the center region.